REMARKS

In view of the amendments proposed above, Applicants respectfully request consideration of the following remarks.

Anticipation Rejections Under 35 U.S.C. § 102

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Brothers v. Union Oil Co. of California*, 2 U.S.P.Q.2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 U.S.P.Q.2d 1913, 1920 (Fed. Cir. 1989).

Anticipation Rejection Based on United States Patent 5,854,638 to Tung

Claims 1, 2, 20, and 21 were rejected under 35 U.S.C. § 102(b) as being anticipated by United States Patent 5,854,638 to Tung (hereinafter "Tung"). Applicants respectfully traverse this rejection as set forth below.

Independent claim 1, as amended, recites:

1.   A method comprising:
        initializing a circuit said circuit having at least one memory element
coupled to a memory bus on a host system;
        monitoring signals on the memory bus;
        detecting a first sequence of signals, the first sequence of signals
including a reserved memory address, **the reserved memory address
comprising a particular memory address reserved for switching control of
the at least one memory element; and**
        switching control of the at least one memory element to the circuit **in
response to detection of the reserved memory address.**

Independent claim 20, as amended, recites some limitations similar to those recited in claim 1 above.

Tung discloses a system and method for implementing a unified memory architecture, wherein the unified memory is divided into at least two memory banks. Column 2, Lines 46-49. Referring to FIG. 1 of Tung, the system includes a host 110 that is coupled via a host bus 112 with host memory controller 114, which in turn is coupled via a memory bus 117 to a unified memory 118. Column 3, Lines 33-43. The unified memory 118 comprises two memory banks, including a host exclusive bank 152 and a shared bank 150, wherein the shared bank 150 is coupled with the host memory controller 114 by a separate shared memory bus 116 and a gate 154. Column 3, Lines 44-64. The system also includes a video controller 126 that is coupled via a video memory bus 128 with the shared memory bank 150, wherein the host memory controller 114 and video controller 126 share control of the shared memory bank 150. Column 4, Lines 14-26. In order for the host memory controller 114 to control the shared memory bank 150, the host memory controller 114 "must engage in arbitration" with the video controller 126. Column 12, Lines 47-49. The arbitration protocol for control of the shared memory bank 150 is described in Tung as follows:

> Under the arbitration protocol used in the present embodiment for control of the shared bank(s) 150, the default owner of the resource is the host memory controller 114. Ownership is transferred to the video controller 126 **in response to a request** therefore, and the video controller 126 returns ownership to the host memory controller 114 **at the end of its activities**, or **in response to a preemption request** by the host memory controller. Column 12, Lines 58-65 (emphasis added).

Thus, Tung discloses a memory arbitration protocol wherein control of a memory may be transferred in response to: (1) a request from a device wanting control of the memory, (2) the end of activities by the device currently controlling the memory, or (3) a host preemption request.

In contrast to Tung, the presently claimed invention is directed to a scheme wherein control of a memory element is switched in response to detection of a reserved memory address on a memory bus, the reserved memory address comprising a particular memory address that has been reserved for switching control of the memory element. Tung fails to disclose such limitations.

As Tung fails to disclose at least the above-noted limitations of claims 1 and 20, each of these claims is novel in view of this reference. Also, claims 2 and 21 are allowable as depending from novel independent claims 1 and 20, respectively.

Anticipation Rejection Based on United States Patent Application Publication US 2002/0199052 to Moyer

Claims 1-41 were rejected under 35 U.S.C. § 102(e) as being anticipated by United States Patent Application Publication 2002/0199052 to Moyer (hereinafter "Moyer"). Applicants respectfully traverse this rejection as set forth below.

Claim 1, as amended, is reproduced above. Each of independent claims 11 and 20, as amended, recites some limitations similar to those recited in claim 1.

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Independent claim 36, as amended, recites:

36.   A method comprising:

monitoring signals on a memory bus, the memory bus coupled with a
memory and a first processor; and

in response to detecting a reserved memory address on the memory
bus, switching control of the memory from the first processor to a second
processor coupled with the memory bus, wherein **the reserved memory
address comprises a particular memory address reserved for switching
control of the memory.**

Moyer discloses a bus arbitration scheme for the global bus of a computer system

that includes – in addition to the global bus (see FIG. 1, item 12) – a CPU 14, system

memory 20, 22, 24, alternate bus masters 36, 38, 40, peripherals 28, 30, and a bus arbiter

34, all coupled with the global bus 12. Moyer, at paragraphs 0017 and 0022 (lines 1-3).

The bus arbiter 34 includes (see FIG. 4) a Logic Circuit 50 coupled with the global bus

12 to receive Current Transfer Type Signals 53. Moyer, at paragraph 0021. Bus arbiter

34 also includes a Policy Select Logic circuit 54 coupled with Logic Circuit 50, wherein

the Policy Select Logic circuit 54 generates an Arbitration Policy signal that is connected

to an input of Logic Circuit 50. Moyer, at paragraph 0021. Moyer goes on to state:

Bus Arbiter 34 uses **information about a current transfer** to make Global Bus
12 control decisions upon receipt of one or more bus requests to use Global Bus
12. When Logic Circuit 50 receives one or more bus requests from any of CPU
14 and Alternate Bus Masters 36, 38, and 40, a decision is made within Logic
Circuit 50 **based upon some predetermined criteria** as to which bus request
should be serviced first.

* * * *

Logic Circuit 50 conditionally asserts the Bus Grant CPU signal or a Bus Grant
signal for one of the requesting Alternate Bus Masters 36, 38, and 40 **based on**

the Current Transfer Type Signals 53 and **information contained in Control
Register** 56. If bus ownership is transferred to a master other than the one
performing the current transfer (i.e. transfer master status from a present or
current communication bus master), the current transfer is interrupted, and a
previously asserted bus grant signal is negated in order to force the Global Bus
12 to be relinquished and thus allow the higher priority master to gain bus
ownership during an on-going burst transfer. Moyer, at paragraph 0022
(emphasis added).

Thus, Moyer discloses a bus arbitration scheme, wherein bus ownership is
assigned based upon: (1) information about the transfer currently taking place on the
global bus; and (2) some predetermined arbitration policy. In the arbitration scheme
disclosed in Moyer, ownership is not transferred in response to detection of a reserved
memory address.

In contrast to Moyer, the present claimed inventions are directed to schemes
wherein control of a memory element is switched in response to detection of a reserved
memory address on a memory bus, the reserved memory address comprising a particular
memory address that has been reserved for switching control of the memory element.
Moyer fails to disclose such limitations.

Each of independent claims 1, 11, 20, and 36 was amended to clarify that a
"reserved memory address" is a "particular memory address reserved for switching
control of the at least one memory element." Support for the claim amendments can be
found in paragraphs [0023] and [0029] of the as-filed specification.

Accordingly, as Moyer fails to teach at least the above-noted limitations of each
of independent claims 1, 11, 20, and 36, each of these claims is novel in view of Moyer.
Also, claims 2-10, 30, and 31, claims 12-19, 32, and 33, claims 21-29, 34, and 35, and

claims 37-41 are allowable as depending from novel independent claims 1, 11, 20, and

36, respectively.

Obviousness Rejections Under 35 U.S.C. § 103

To reject a claim or claims under 35 U.S.C. § 103, the Examiner bears the initial

burden of establishing a prima facie case of obviousness. M.P.E.P. § 2142. When

establishing a prima facie case of obviousness, the Examiner must set forth evidence

showing that the following three criteria are satisfied:

> First, there must be some suggestion or motivation, either in the references
> themselves or in the knowledge generally available to one of ordinary skill in
> the art, to modify the references or to combine teachings. Second, there must
> be a reasonable expectation of success. Finally, the prior art references (or
> references when combined) must teach or suggest all the claim limitations.
> M.P.E.P. § 2143.

The teaching or suggestion to make the claimed combination and the reasonable

expectation of success must both be found in the prior art, and not based on the

applicant's disclosure. M.P.E.P. § 2142 (citing *In re Vaeck*, 20 U.S.P.Q.2d 1438 (Fed.

Cir. 1991)). Also, the evidentiary showing of a motivation or suggestion to combine

prior art references "must be clear and particular." *In re Dembiczak*, 175 F.3d 994, 999,

50 U.S.P.Q.2d 1614, 1617 (Fed. Cir. 1999).

Obviousness Rejection Based on United States Patent Application Publication US 2002/0199052 to Moyer

Claims 42-43 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Moyer. Applicants respectfully traverse this rejection as set forth below.

As set forth above, Moyer fails to disclose all limitations of independent claim 36 and, therefore, claim 36 is patentable in view of Moyer. If an independent claim is nonobvious, then any claim depending from the independent claim is also nonobvious. M.P.E.P. §2143.03 (citing *In re Fine*, 5 U.S.P.Q.2d 1596 (Fed. Cir. 1988)). Therefore, claims 42 and 43 are allowable as depending from nonobvious, independent claim 36.

CONCLUSION

Applicants submit that claims 1-43 are in condition for allowance and respectfully request allowance of such claims.

Please charge any shortages and credit any overages to our Deposit Account No. 02-2666.

Respectfully submitted,

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